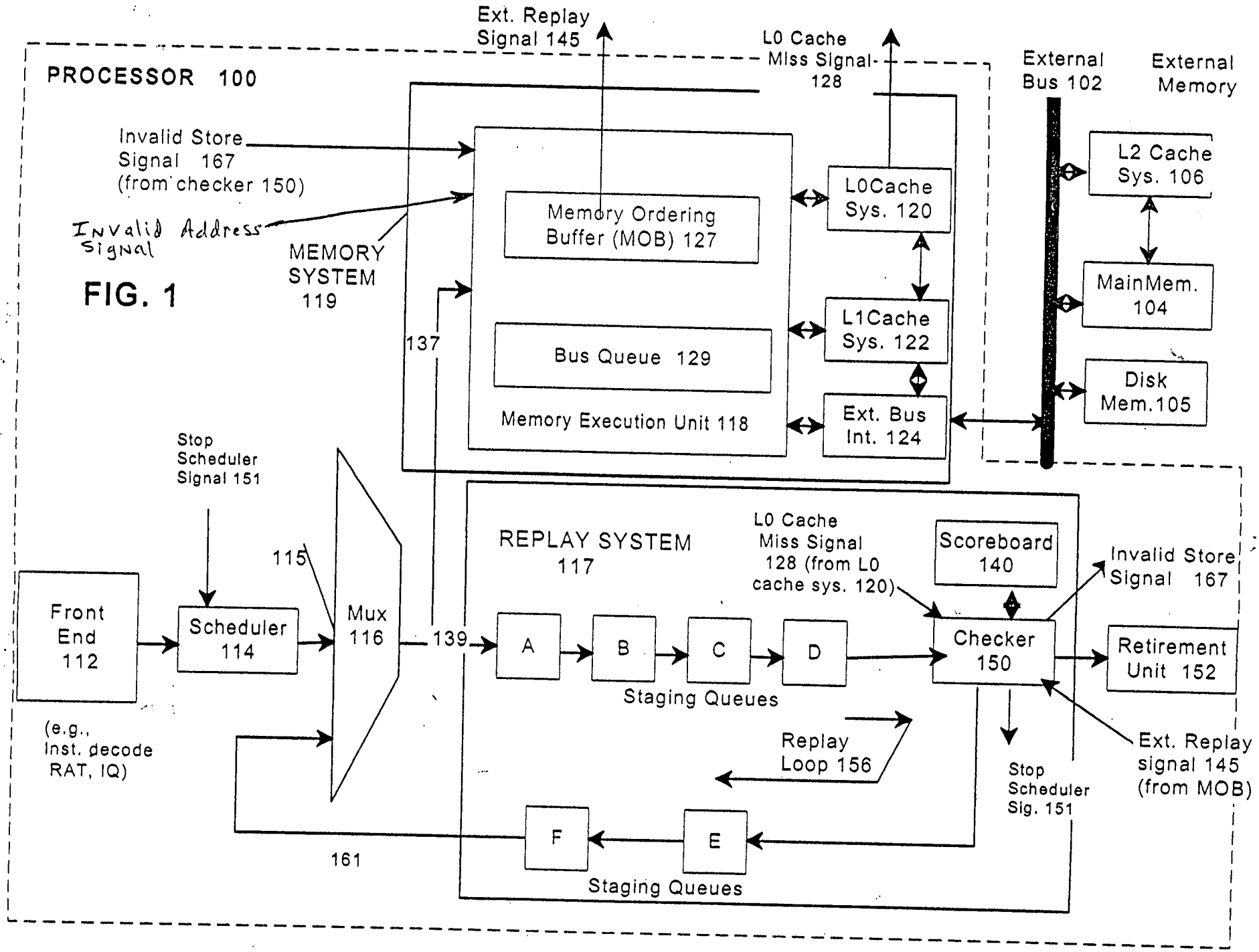

PROCESSOR 100
Ext. Replay Signal 145
L0 Cache Miss Signal 128
External Bus 102
External Memory
Invalid Store Signal 167 (from checker 150)
Invalid Address Signal
MEMORY SYSTEM 119
Memory Ordering Buffer (MOB) 127
L0Cache Sys. 120
L2 Cache Sys. 106
MainMem. 104
L1Cache Sys. 122
Disk Mem.105
Bus Queue 129
Memory Execution Unit 118
Ext. Bus Int. 124
137
Stop Scheduler Signal 151
115
REPLAY SYSTEM 117
L0 Cache Miss Signal 128 (from L0 cache sys. 120)
Scoreboard 140
Invalid Store Signal 167
Front End 112
Scheduler 114
Mux 116
139
A
B
C
D
Checker 150
Retirement Unit 152
Staging Queues
(e.g., Inst. decode RAT, IQ)
Replay Loop 156
Stop Scheduler Sig. 151
Ext. Replay signal 145 (from MOB)
F
E
161
Staging Queues

FIG. 1

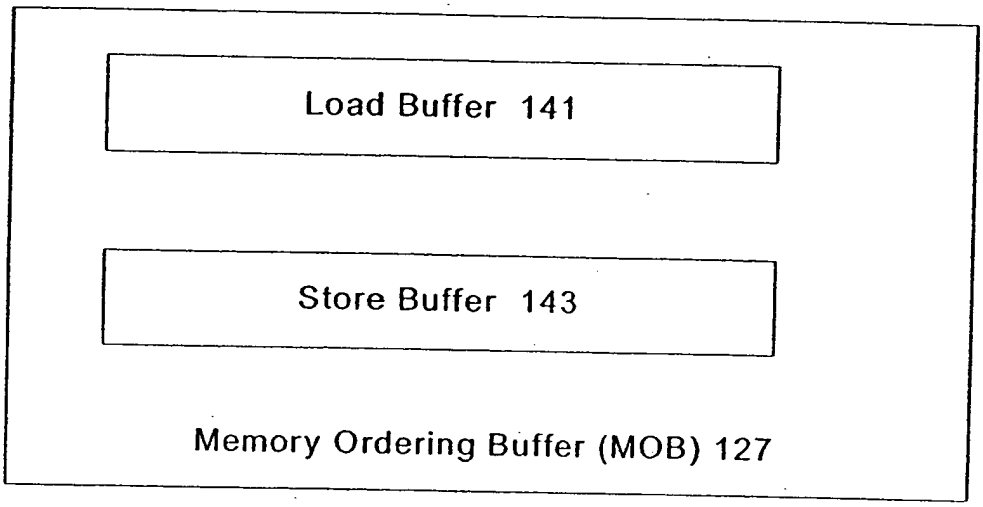
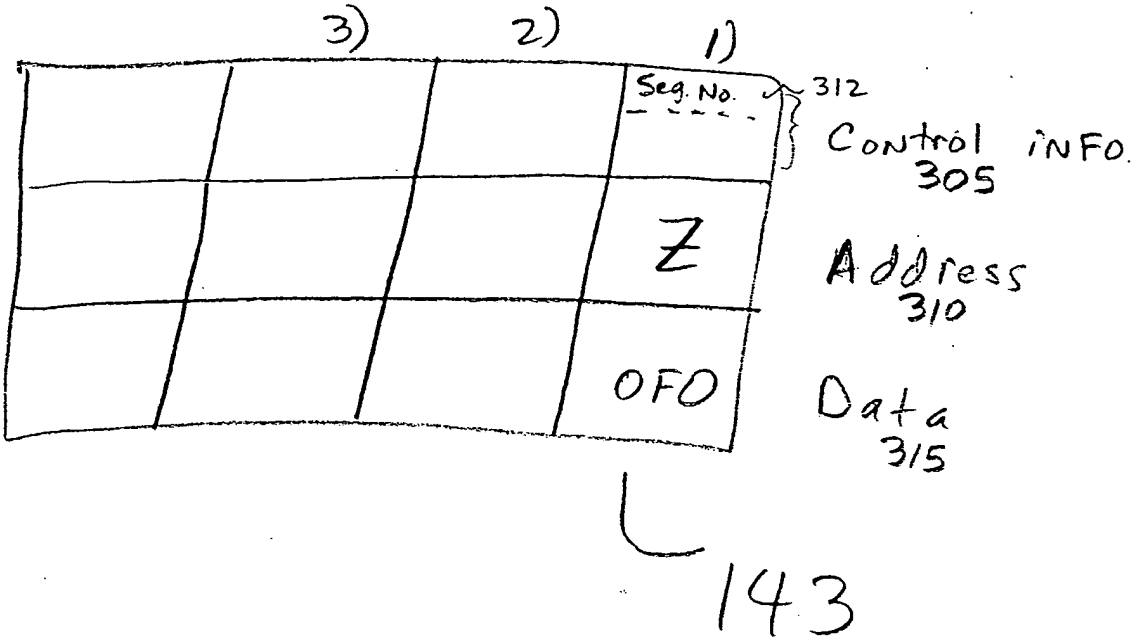

Load Buffer 141
Store Buffer 143
Memory Ordering Buffer (MOB) 127

Fig. 2

Store Buffer



Load Buffer

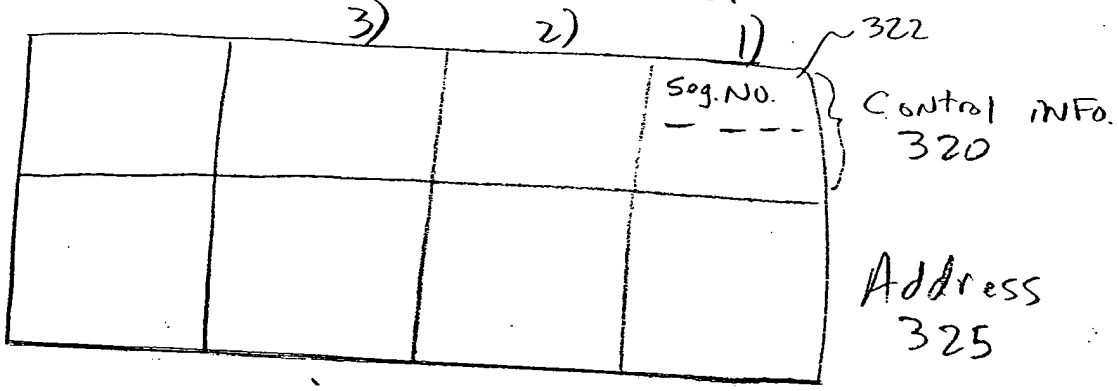


Fig. 3

Operation	SRC	Dest
1) Store	R4,	[R1]
2) Load	[X],	R2

Reg.	Correct Value	Incorrect Value
R_1	X	Y

L0 Cache System 120

Addr.	Data
X	F000

Fig. 4

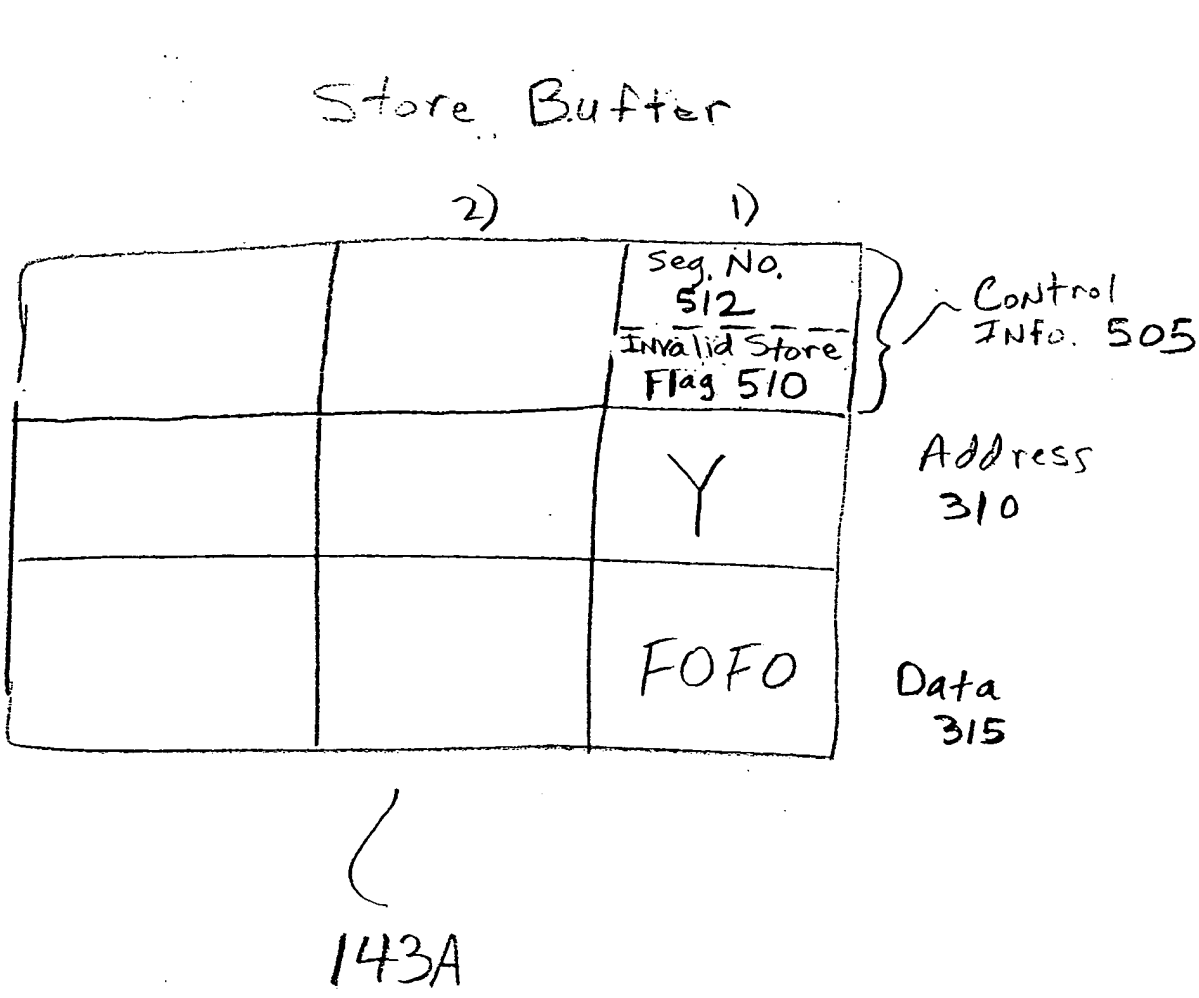

Store Buffer
2)
1)
Seg. No. 512
Invalid Store Flag 510
Control Info. 505
Y
Address 310
FOFO
Data 315
143A

Fig. 5

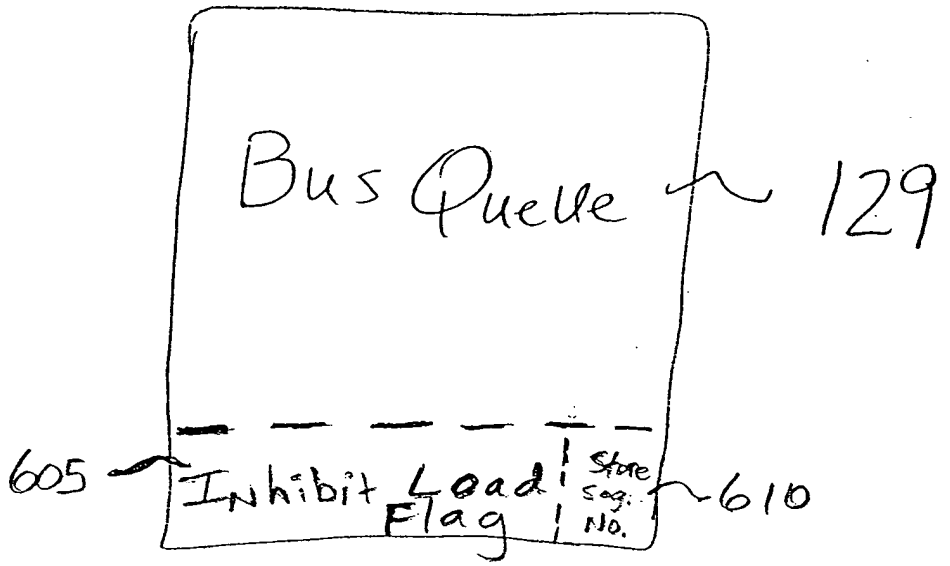


Fig. 6

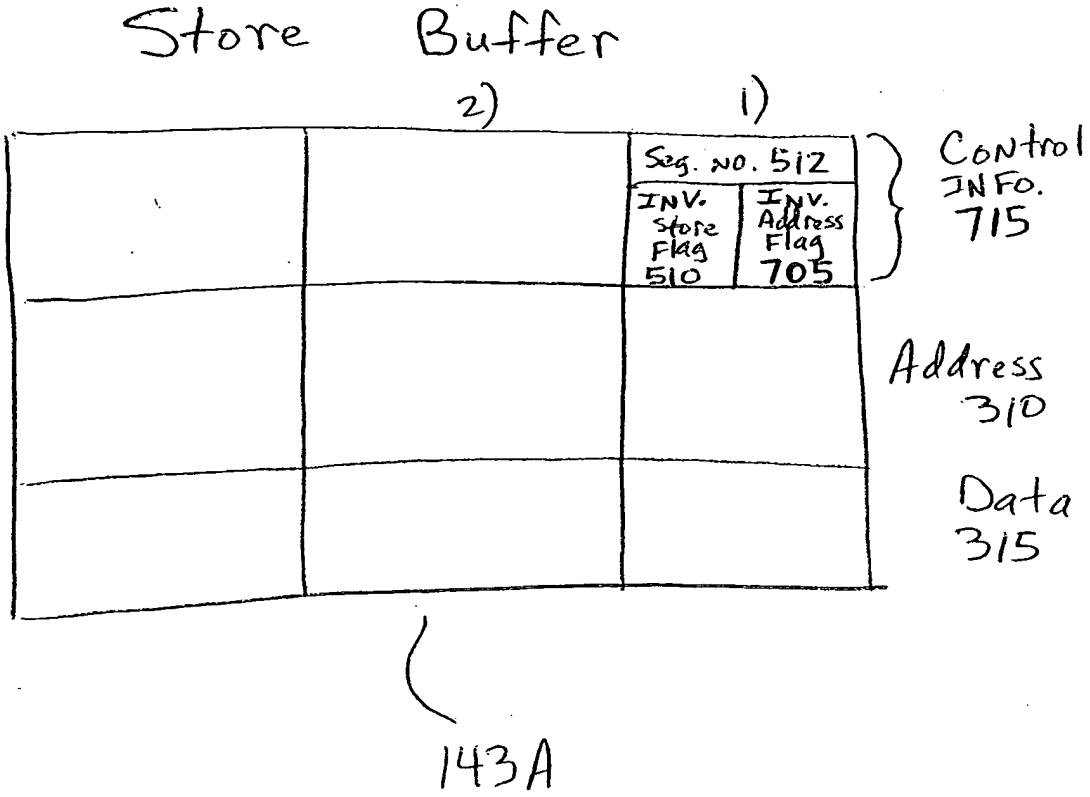

Store Buffer
2)
1)
Seg. no. 512
INV. Store Flag 510
INV. Address Flag 705
Control INFO. 715
Address 310
Data 315
143A

Fig. 7